## REMARKS

Claims 1-14 were pending in this application, of which claims 1, 2, 3, 6, 7, and 9-14 have been rejected and claims 4, 5, and 8 have been withdrawn from consideration. Upon entry of the following amendments, claims 1-3, 6-7, and 9-14 will remain pending in this application and claims 15-16 will be added. The amendments to the claims are fully supported by the specification and the original claims. No new matter has been incorporated by this Amendment. The Examiner is respectfully requested to reconsider and withdraw the outstanding rejections and objections in view of the amendments and remarks contained herein.

### OBJECTION TO CLAIM

As amended, claim 1 has been corrected to remove the informality, noted by the Examiner, in the last two lines of the claim.

### OBJECTION UNDER 37 CFR 1.83(a)

The drawings were objected to under 37 CFR 1.83(a) for failure to show every feature of the invention specified in the claims. Specifically, the Examiner asserts that the drawings lack the dual amplifier embodiment that combines the amplifier structure with a gate and the amplifier structure with a base as claimed in claim 11. However, by this Amendment, claim 11 now depends from claim 9, and this combination is no longer a claimed feature. Therefore, Applicants respectfully submit that this objection is traversed without the need for change to the drawings.

**REJECTION UNDER 35 U. S. C. § 102**

Claims 1, 2, 3, 6, 7, 9, and 12 were rejected under 35 U. S. C. § 102(b) as allegedly anticipated by Miguelez et al. (U.S. Patent No. 6,107,877). Applicants respectfully submit that the rejection should be withdrawn because the cited patent fails to inherently or explicitly disclose every feature detailed in the amended claims.

Except for new dependent claim 16, the active dependent claims (claims 2, 3, 6, 7, 9, and 12 included) now dependent from both amended claim 1, and new independent claim 15. As such claims 1 and 15 will be discussed, in turn, in regard to Miguelez. We will begin with claim 1.

Amended claim 1 recites the following feature: a specific-frequency suppressing means suppresses all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to the input terminal. Miguelez fails to teach or suggest this feature. According to Applicants, Miguelez discloses capacitor 111 (see Figs 6 and 7 of Miguelez) with an impedance that is much higher, for all or part of the frequencies, than the range – from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal – recited in amended claim 1. As such, Applicants respectfully submit that, as amended, independent claim 1 is not anticipated by Miguelez under 35 U.S.C. §102 and rather is in condition for allowance thereover.

Independent claim 15 recites the following feature: a specific-frequency suppressing means suppresses at least one higher harmonic frequency of a carrier wave of the input signal. This recitation in claim 15 places limits on the impedance of the specific-frequency suppressing means as viewed from the connection point to which the specific-frequency suppressing means is

connected (cf. claim 2). To those of ordinary skill in the art, however, Miguelez would not have taught or suggested such limits on impedance. According to Applicants, in Miguelez, the composite impedance of capacitor 111 and resistor 112 corresponds to the impedance "viewed from the connection point to which the specific-frequency suppressing means is connected". Further according to Applicants, this impedance in Miguelez cannot be sufficiently low because of the resistor 112, even if the impedance of capacitor 111 is much lower. Miguelez, therefore, fails to teach or suggest the structure described in independent claim 15.

**REJECTION UNDER 35 U. S. C. § 103**

Claims 10, 11, 13, and 14 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Miguelez (previous cite) in view of Yun et al. (U.S. Patent No. 5,914,641) and Fukuden (U. S. Patent No. 5,805,023). Applicants respectfully submit that this rejection should be withdrawn in light of this amendment of claim 1 and addition of claim 15.

Applicants submit that the present invention as set forth in either claim 1 or claim 15 is not made obvious by Miguelez singly, or in any combination with Yun and Fukuden. Neither Yun nor Fukuden remedies the above-described deficiencies of Miguelez with respect to claims 1 and 15. Therefore, claims 10, 11, 13, and 14 which depend from claims 1 and 15 are likewise patentably distinguishable over Miguelez, Yun and Fukuden. Moreover, it is respectfully submitted that there is nothing in the cited documents that would have motivated those of ordinary skill in the art to have combined the teachings of the cited art in any way that would render the claimed invention obvious. As such, Applicants respectfully urge that the asserted rejection over the alleged combinations of Miguelez, Yun and Fukuden are overcome.

## CONCLUSION

Applicants respectfully submit that this Amendment and the above remarks obviate the outstanding rejections and objections in this case, thereby placing the application in condition for immediate allowance. Allowance of this application is earnestly solicited.

If any fees under 37 C. F. R. §§ 1.16 or 1.17 are due in connection with this filing, please charge the fees to Deposit Account No. 02-4300, Order No. 033216M067.

Respectfully submitted,
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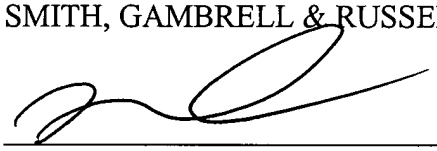
By: 

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Dated: July 22, 2003

## Listing of Claims

1. (Twice Amended) A predistortion circuit comprising:

an input terminal for inputting a predetermined signal;

a nonlinear device directly or indirectly connected to said input terminal;

~~A~~ a bias supply circuit for applying a voltage to said nonlinear device;

specific–frequency suppressing means connected to one side or both sides of said nonlinear device directly without another intervening device, said specific–frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width ~~on in~~ of an input signal inputted to said input terminal ~~and/or suppressing at lest one higher harmonic frequency of a carrier wave of said input signal~~; and

an output terminal for outputting a signal.

2. (Twice Amended) A predistortion circuit of Claim 1 or 15, wherein said specific–frequency suppressing means has such impedance that the impedance of said specific–frequency suppressing means viewed from the connection point to which said specific–frequency suppressing means is connected is lower than the impedance of said nonlinear device viewed from said connection point at all or part of such frequencies that are from said frequency corresponding to DC to said frequency corresponding to said occupied band width and/or at least one higher harmonic frequency of a carrier wave of said input signal.

3. (Currently Amended) A predistortion circuit of Claim 1 or 15, wherein said nonlinear device is provided between the connection point between said input terminal and said output terminal and the ground.

4. (Withdrawn)

5. (Withdrawn)

6. (Currently Amended) A predistortion circuit of ~~any one of Claims~~ Claim 1 ~~to 5~~ or 15, wherein said specific-frequency suppressing means comprises the all or part of a resistor, a coil, a capacitor, and a transmission line.

7. (Currently Amended) A predistortion circuit of ~~any one of Claims~~ Claim 1 ~~to 4~~ or 15, wherein said nonlinear device comprises a diode.

8. (Withdrawn And Currently Amended) A predistortion circuit of ~~any one of Claims 1 to 4~~ Claim 1, wherein said nonlinear device comprises a transistor.

9. (Currently Amended) A power amplifier comprising: a predistortion circuit of ~~any one of Claims~~ Claim 1 ~~to 5~~ or 15; and an amplifier for amplifying the signal from said predistortion circuit.

10. (Previously Amended) A power amplifier of Claim 9, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the gate of which is connected to said first matching circuit;

a second matching circuit connected to the drain of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific–frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device, said specific–frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

11. (Twice Amended) A power amplifier of Claim ~~10~~ 9, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the base of which is connected to said first matching circuit;

a second matching circuit connected to the collector of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific–frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device, said specific–frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

12. (Currently Amended) A predistortion circuit of ~~claim 6~~ claim 1 or 15, wherein said specific–frequency suppressing means is composed of lumped parameter components interconnected in series.

13. (Previously Added) A predistortion circuit of claim 6, wherein said specific–frequency suppressing means is composed of a transmission line.

14. (Previously Added) A predistortion circuit of claim 6, wherein said specific–frequency suppressing means is composed of a transmission line and a capacitor interconnected in series.

15. (New) A predistortion circuit comprising:

an input terminal for inputting a predetermined signal;

a nonlinear device directly or indirectly connected to said input terminal;

a bias supply circuit for applying a voltage to said nonlinear device;

specific–frequency suppressing means connected to one side or both sides of said nonlinear device directly without another intervening device, said specific–frequency suppressing means suppressing at least one higher harmonic frequency of a carrier wave of said input signal; and

an output terminal for outputting a signal.

16. (New) A predistortion circuit of Claim 15, wherein said one higher harmonic frequency is the second harmonic frequency.

Abstract of the Disclosure

A predistortion circuit has an input terminal for inputting a predetermined signal; a nonlinear device directly or indirectly connected to the input terminal; a bias supply circuit for applying a voltage to the nonlinear device; a specific-frequency suppressing device connected to one side or both sides of the nonlinear device directly without another intervening device for suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to the input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of the input signal; and an output terminal for outputting a signal.